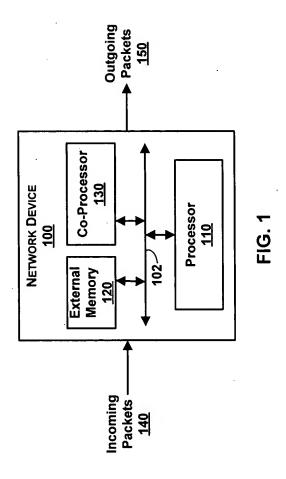Express Mail Label No. EV 333134808 US
Title: Instruction Memory Hierarchy In An
Embedded Processor
Inventor: Donald E. Steiss
Atty. Docket No.: 22347-08261 (8117)
Sheet 1 of 7

FIG. 1

Express Mail Label No. EV 333134808 US
Title: Instruction Memory Hierarchy In An
Embedded Processor
Inventor: Donald E. Steiss
Atty. Docket No.: 22347-08261 (8117)
Sheet 2 of 7

FIG. 2

Express Mail Label No. EV 333134808 US
Title: Instruction Memory Hierarchy In An
Embedded Processor
Inventor: Donald E. Steiss
Atty. Docket No.: 22347-08261 (8117)
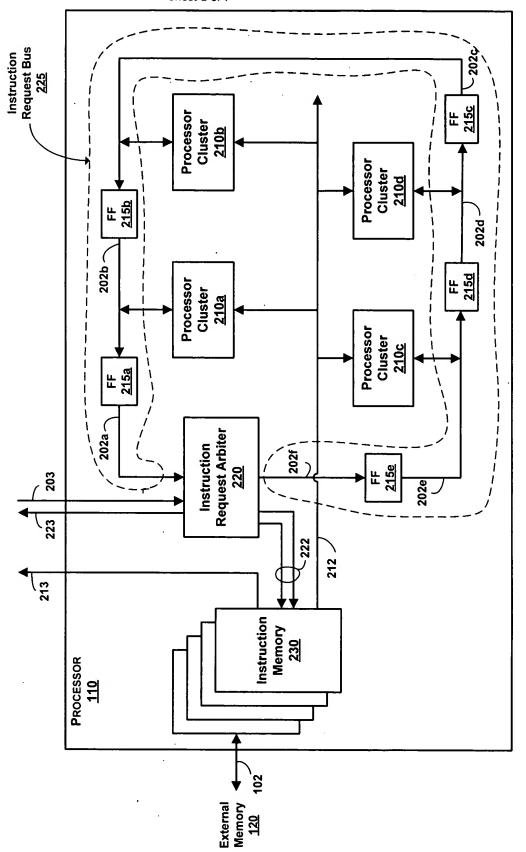Sheet 3 of 7

300

External Memory
120

102

Instruction
Memory
230

222

Instruction
Request Arbiter
220

212

225

PROCESSOR CLUSTER
210

302

Processing Unit
310b

Cache
312b

Processing Unit
310d

Cache
312d

Processing Unit
310a

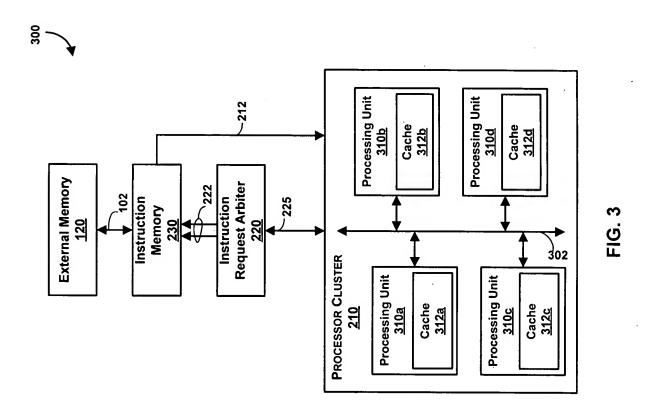Cache
312a

Processing Unit
310c

Cache
312c

FIG. 3

Express Mail Label No. EV 333134808 US
Title: Instruction Memory Hierarchy In An
Embedded Processor
Inventor: Donald E. Steiss
Atty. Docket No.: 22347-08261 (8117)
Sheet 4 of 7
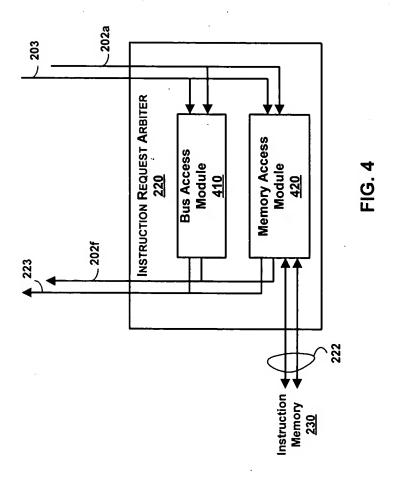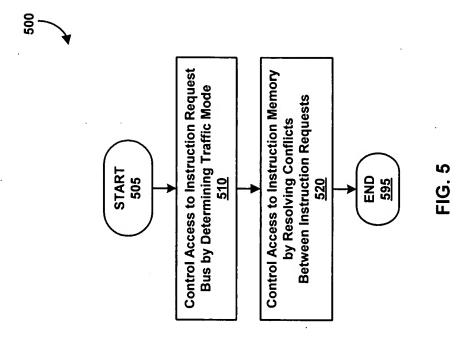
FIG. 4

Express Mail Label No. EV 333134808 US
Title: Instruction Memory Hierarchy In An
Embedded Processor
Inventor: Donald E. Steiss
Atty. Docket No.: 22347-08261 (8117)
Sheet 5 of 7

500

START
505

Control Access to Instruction Request
Bus by Determining Traffic Mode
510

Control Access to Instruction Memory
by Resolving Conflicts
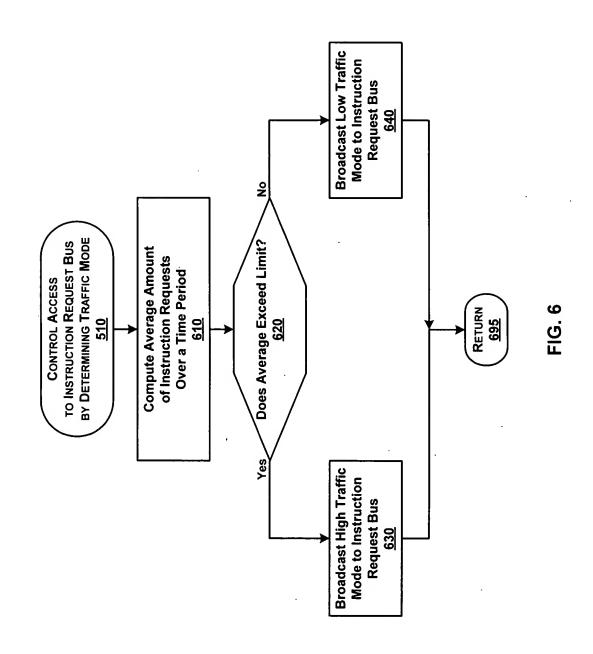Between Instruction Requests
520

END
595

FIG. 5

Express Mail Label No. EV 333134808 US
Title: Instruction Memory Hierarchy In An
Embedded Processor
Inventor: Donald E. Steiss
Atty. Docket No.: 22347-08261 (8117)
Sheet 6 of 7

CONTROL ACCESS
TO INSTRUCTION REQUEST BUS
BY DETERMINING TRAFFIC MODE
510

Compute Average Amount
of Instruction Requests
Over a Time Period
610

Does Average Exceed Limit?
620

No

Yes

Broadcast Low Traffic
Mode to Instruction
Request Bus
640

Broadcast High Traffic
Mode to Instruction
Request Bus
630

RETURN
695

FIG. 6

Express Mail Label No. EV 333134808 US
Title: Instruction Memory Hierarchy In An
Embedded Processor
Inventor: Donald E. Steiss
Atty. Docket No.: 22347-08261 (8117)
Sheet 7 of 7

CONTROL ACCESS
TO INSTRUCTION MEMORY BY
RESOLVING CONFLICTS BETWEEN
INSTRUCTION REQUESTS
520

Receive Instruction Requests from
Processor Clusters
710

Any Conflicting
Instruction Requests?
720

No

Forward Instruction
Requests
760

Yes

Do Conflicting Request
Have the Same Priority?
730

Forward Selected
Instruction Request
Using Round-Robin
Arbitration
750

Select High Priority
Instruction Request
740

RETURN
795

FIG. 7